**Home Assignment 3**

**ECSE108L Digital Design**

1. Simplify the following Boolean function F, together with the don’t-care conditions d.
   1. F (A,B,C,D) = ∑(0, 6, 8 13, 14)

d(A,B,C,D) = ∑(2,4,10)

* 1. F (A,B,C,D) = ∑(2,4,7, 10,12)

d(A,B,C,D) = ∑(0,6,8)

1. Draw the logic diagram for the following Verilog description and convert into behavioural Verilog code

**module** Circuit\_A (A, B, C, D, F);

**input** A, B, C, D;

**output** F;

**wire** w, x, y, z, a, d;

**or** (x, B, C, d);

**and** (y, a ,C);

**and** (w, z ,B);

**and** (z, y, A);

**or** (F, x, w);

**not** (a, A);

**not** (d, D);

**endmodule**

1. Design 4 bit adder subtractor that can handle both the cases.
2. Analyze 4 bit ripple carry adder and carry lookahead adder in terms of execution time and in terms of gate input(G) and gate input with not(GN).
3. Design 4-16 Decoder using 2-4 decoder with enable.
4. Design 16-1 MUX using 4-1 MUX.
5. Design 1-8 DMUX using 1-4 and 1-2 DMUX.
6. Design a circuit Perform following operation using only **one full adder and 4-1 MUX and 1-4 DMUX**. Here a, b, c, d, e are input and Y is output.

b

a

Y

e

d

c